REMARKS

I. Present Disposition of the Claims

Applicants wish to reiterate thanks to the Examiner for the useful comments in the Telephonic Interview on July 31, 2003, and the final Office Action dated July 22, 2003. Claims 1-4, 6-14, and 16-20 are pending in the application. Claims 1-4, 6-14, and 16-20 are rejected in the application. Independent Claims 1 and 11 have been herein amended and dependent Claims 5 and 15 have been previously canceled, without prejudice.

Specifically, independent Claims 1 and 11 are herein amended by adding the underlined limitations that the Cu-Zn allow fill in the via is directly deposited on the Cu surface and that the Cu-Zn alloy fill having an alloy surface and an alloy thickness and having a uniform zinc distribution across said alloy surface and said alloy thickness. Claims 1 and 11 are fully supported by the Specification, i.e., p. 12, ll. 6-9, and are believed to be in allowable form. No new matter has been added with this amendment. Therefore, reconsideration of the present application in light of the foregoing proposed amendment and these remarks is respectfully requested.

I. Rejection of Claims 1 and 11 under 35 U.S.C. § 112

Claims 1 and 11, under 35 U.S.C. § 112, second paragraph, have been rejected as being indefinite due to ambiguity of the location of the uniform zinc distribution. Applicants respectfully traverse this rejection. In light of the Examiner's rejection, Applicants have amended Claims 1 and 11 to reflect that a Cu-Zn alloy fill has a uniform zinc distribution across an alloy fill surface and an alloy thickness (underlining added for emphasis of added limitations). As such, the Office Action rejection should be moot. Thus, Applicants respectfully request that the Examiner's rejection be withdrawn.

II. Rejection of Claims 1-4, 10-14 and 16 under 35 U.S.C. § 103(a)

Claims 1-4, 10-14 and 16, under 35 U.S.C. § 103(a), are rejected as being unpatentable over Krishnamoorthy et al. (US 6,486,533) ("Krishnamoorthy"), in view of Miyafuji et al. (US 6,313,064) ("Miyafuji"), stating:

> .. one of ordinary skill in the art would have recognized post annealed Cu-Zn alloy is nothing but the reduced-oxygen Cu-Zn alloy, in light of the teachings of Miyafuji et al.. In particular, Miyafuji et al. in an analogous art of Cu-Zn alloy formation suggest that by subjecting the Cu-Zn alloy to a heat treatment (i.e. the annealing) at the proper temperature the Zn in the Cu-Zn would oxidize as ZnO due to the fact that Zn has far more intense affinity with oxygen than Cu. In other words, by subjecting to the heat treatment (i.e. the annealing) oxygen concentration in the Cu-Zn alloy would reduce, i.e. producing the reduced-oxygen Cu-Zn alloy. Therefore , it would have been obvious to one of ordinary skilled in the art, at the time the invention was made to, appreciate that the post-annealed Cu-Zn alloy of Krishnamoorthy et al. is the reduced-oxygen Cu-Zn alloy, since it is an inherent consequence of the annealing, as evidenced by Miyafuji et al.

Notwithstanding independent Claims 1 and 11 being herein amended as discussed above, Applicants respectfully traverse the Examiner's rejection. Further, dependent Claims 2, 3, 4, 10, 12, 13, 14 and 16 subsume the limitations of their respective independent Claims 1 and 11 from which they depend.

The Manual for Patent Examiners' Practice paragraph 2142 addresses the 103(a) basis for rejection, mandating that ". . . To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), MPEP Section 706.02(j). "Mere fact that prior art may be modified to reflect features of claimed invention does not make modification, and hence claimed invention, obvious unless desirability of such modification is suggested by prior art . . .", *In re Fritch*, 922 F.2d 1260, 23 USPQ.2d 1780, at p. 1780 (Fed. Cir. 1992).

First, the primary reference Krishnamoorthy provides a solution for the electronic industry to prevent copper integrated structures becoming oxidized and non electrically conductive (Col. 2, ll. 24-25, ll. 31-32). The secondary reference Miyafuji provides a solution to create an antibacterial effect and sterilizing effect for copper when irradiated by UV light for the express need to produce a clean environment in hallways and meeting rooms (Col 1 , ll. 4-6; Col. 3; ll. 7-8). Thus, primary cited reference Krishnamoorthy Cu-Zn alloy methodology for integrated circuits does not provide a motivation to seek a secondary reference Miyafuji that provides Cu

surface sterilization for hallways and buildings. Second, there is not a reasonable expectation of successful combination of the cited references because Krishnamoorthy Cu-Zn alloy techniques for electronic circuit conductivity improvement may or may not work with Miyafuji Cu sterilization techniques. Third, as stated in the Office Action, the references do not teach nor suggest the limitations of herein amended Claims 1 and 11 because as stated in the Office Action, "Krishnamoorthy is silent as to post annealed Cu-Zn alloy being claimed reduced-oxygen Cu-Zn alloy." As such, Krishnamoorthy does not teach, suggest, nor motivate a reasonable expectation of success that its Cu-Zn alloy will combine with secondary cited reference Miyafuji Cu sterilization method. Therefore, the references cited to reject Applicants claims do not in fact provide an adequate basis for rejection under 35 U.S.C. § 103(a). Thus, Applicants respectfully request the rejections be withdrawn and Claims 1 and 11 pass to allowance.

Further, the Office Action states:

> In re claim 1, Krishnamoorthy et al. teach the claimed method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:
> - providing a semiconductor substrate having a Cu surface 35 (i.e. a bonding layer; col. 4, lines 60-64) formed in a via (Fig.1);
> - providing a chemical solution (i.e. an electroplating solution);
> - electroplating the Cu surface 35 in the chemical solution, thereby forming a Cu-Zn alloy 40 fill in the via and on the Cu surface 35 in the chemical solution, thereby
> - rinsing the Cu-Zn alloy fill 40 in a solvent stored in a rinsing chamber (col. 9, lines 33-37)
> - drying the Cu-Zn fill 40 under a gaseous flow (col. 9, lines 33-44);
> - annealing the Cu-Zn alloy fill 40 formed in the via and on the Cu surface 35 (col. 5, line 61 and col.6, line 6), thereby forming a post-annealed Cu-Zn alloy fill;
> - planarizing the post-annealed Cu-Zn alloy fill and the Cu surface 35, thereby completing formation of the post-annealed Cu-Zn alloy filled dual-inlaid interconnect structure (Fig.1); and
> - completing formation of the semiconductor device.
>
> Krishnamoorthy et. al. is silent as to the post-annealed Cu-Zn alloy being the claimed reduced-oxygen Cu-Zn alloy.

Contrary to the present invention, the first cited reference Krishnamoorthy teaches against herein amended independent Claims 1 and 11 limitation "a Cu-Zn alloy fill in the via is **directly deposited** on the Cu surface." Specifically, Krishnamoorthy teaches a method for forming microelectronic metallized structures wherein a dielectric layer 25 provides a foundational layer for depositing an ultra-thin film bonding layer 35 and a low-Me concentration, copper-zinc, alloy layer 40. Further, Krishnamoorthy recites "[a] metallized structure 20 is comprised of an ultra-

thin bonding layer 35 disposed exterior **to the dielectric layer 25**, a low-zinc concentration, copper-zinc alloy layer 40 disposed exterior to **the ultra-thin bonding layer 35**, and an optional primary conductive layer 45 disposed exterior to the copper-zinc alloy layer 40" (Col. 4, ll. 30-42; Exhibit B). The **dielectric layer is the foundational layer** for the Krishnamoorthy metallization scheme (Col. 4, ll. 13-27):

> The composition of the dielectric layer 25 is generally dependent on the function of the metalization structure 20. When the metalization structure 20 is used to implement a post or line of an electrical interconnect network, the dielectric layer 25 is preferable comprised of a low-K material. When the metalization structure is used to implement a discrete microelectronic component such as a capacitor, however, the dielectric layer 25 is preferably comprised of a high-K material. To increase adhesion between the dielectric layer 25 and a subsequent layer, such as ultra-thin bonding layer (35), the surface of the dielectric layer may be subject o an adhesion promoting process. For example, the dielectric layer surface may be subject to treatment in an atmosphere having a high ozone content. Alternatively, some form of mild mechanical or chemical abrading process may be used.

Stated differently, the metallization structure described in Krishnamoorthy teaches a **specific dielectric, i.e., non-electrically conductive or insulating, foundational material layer**, as exemplified in the above duplicated passage. Further,"**[t]he bonding layer 35 functions principally as an adhesion promoter to bond the copper-zinc alloy layer 40 to the dielectric layer 25**" (Col. 4, ll. 47-50). As such, **Krishnamoorthy teaches against the present invention independent Claims 1 and 11 of direct bonding of the Cu-Zn alloy layer 30 to a Cu surface 20** (Exhibit A, Fig. 2). As such, independent Claims 1 and 11 limitations of direct depositing the Cu-Zn alloy on the Cu surface 20 is not taught, suggested, nor motivated by Krishnamoorthy.

The secondary cited reference Miyafuji merely teaches diffusion of oxygen into Cu to produce a sterilized Cu alloy surface. Specifically, Miyafuji merely teaches "[O]xygen is diffused into the copper alloy, and thus the alloy can be industrially produced in such a manner that the **amount or size of the produced oxides, the depth of the oxidized layer**, and the like are controlled by combining heating atmosphere (oxygen partial pressure), heating temperature and heating time appropriately" (Col. 4, ll. 63-68; Col. 5, ll. 1-5; Exhibit C). These steps mainly produce ZnO at the surface layer, so that when the surface layer is irradiated with UV light, the surface layer provides **an optical catalyst function that sterilizes the surface layer** (Col 4, ll. 8-12).

In other words, Krishnamoorthy, even in view of Miyafuji, would create **a copper alloy that has optical catalyst function at the surface layer when exposed to light** where the copper alloy contains **oxide particles of various diameters, depending on the diffusion depth of the oxygen.** For example, Fig. 1 (Exhibit C) **shows titanium oxide particles at the surface larger than titanium oxide particles at a depth below the surface** (Fig. 1, Exhibit C). In contrast, herein amended independent Claims 1 and 11 positively recites a method, including the steps of rinsing and drying the substrate, for **the production of a reduced-oxygen Cu-Zn alloy fill 30 having a uniform zinc distribution along the alloy fill thickness**, as indicated by block 2006 (Specification, p. 11, ll. 29-30).

Thus, Krishnamoorthy, even in view of Miyafuji, does not teach, motivate, nor suggest herein amended independent Claims 1 and 11, respectively reciting:

1. **(currently amended)** A method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:
providing a semiconductor substrate having a Cu surface formed in a via;
providing a chemical solution;
electroplating the Cu surface in the chemical solution thereby forming said a Cu-Zn alloy fill in the via and on the Cu surface,
wherein said electroplating comprises using an electroplating apparatus,
wherein said electroplating apparatus comprises:
(a) a cathode-wafer;
(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;
drying the Cu-Zn alloy fill under a gaseous flow;
annealing the Cu-Zn alloy fill formed in the via and **directly deposited on the Cu surface**, thereby forming a reduced-oxygen Cu-Zn alloy fill having **an alloy surface and an alloy thickness and having across said alloy surface and said alloy thickness a uniform zinc distribution**;
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

11. **(currently amended)** A semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by a method comprising the steps of:
providing a semiconductor substrate having a Cu surface formed in a via;
providing a chemical solution;
electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface;

wherein said electroplating comprises using an electroplating apparatus,
wherein said electroplating apparatus comprises:
(a) a cathode-wafer;
(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;
drying the Cu-Zn alloy fill under a gaseous flow;
annealing the Cu-Zn alloy fill formed in the via and **directly deposited on the Cu surface,** thereby forming **an alloy surface and an alloy thickness and having across said alloy surface and said alloy thickness a uniform zinc distribution;**
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

As such, Krishnamoorthy, even in view of Miyafuji, does not teach, motivate, nor suggest the dependent Claims 2, 3, 4, 10, 12, 14, and 16, now subsuming the limitations of the herein amended independent Claims 1 and 11. Therefore, Applicants respectfully request that the Examiner's rejection be withdrawn and the claims pass to allowance.

III. Rejection of Claims 1, 2, 4, 6, 7, 11, 12, 14, 16 and 17 under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1, 2, 4-7, 11, 12, and 14-17, under 35 U.S.C. § 103(a), as being unpatentable over Chen et al. (US 2002/008034 A1) ("Chen"), in view of Miyafuji et al. (US 6,313,064) ("Miyafuji"), stating:

> [ ] one of ordinary skill in the art would have recognized post annealed Cu-Zn alloy is nothing but the reduced-oxygen Cu-Zn alloy, in light of the teachings of Miyafuji et al.. In particular, Miyafuji et al. in an analogous art of Cu-Zn alloy formation suggest that by subjecting the Cu-Zn alloy to a heat treatment (i.e. the annealing) at the proper temperature the Zn in the Cu-Zn would oxidize as ZnO due to the fact that Zn has far more intense affinity with oxygen than Cu. In other words, by subjecting to the heat treatment (i.e. the annealing) oxygen concentration in the Cu-Zn alloy would reduce, i.e. producing the reduced-oxygen Cu-Zn alloy. Therefore , it would have been obvious to one of ordinary skilled in the art, at the time the invention was made to, appreciate that the post-annealed Cu-Zn alloy of Chen et al., is the reduced-oxygen Cu-Zn alloy, since it is an inherent consequence of the annealing, as evidenced by Miyafuji et al.

Notwithstanding independent Claims 1 and 11 are being herein amended, the Applicants respectfully traverse the Examiner's rejection.

See supra, The Manual for Patent Examiners' Practice paragraph 2142 requirements for the 103(a) basis for rejection. First, Chen provides a solution for enhancing or repairing ultra-thin or incomplete metal seed layers that have been deposited on the workpiece. Second, Miyafuji, as discussed previously, provides a solution for providing clean environment Cu alloy

surfaces where UV light irradiating the Cu alloy surface in hallways sterilizes the Cu alloy surface. Thus, Chen providing a solution for enhancing or repairing ultra-thin metal layers does not motivate one to search for the cited reference Miyafuji providing sterilized Cu alloy surfaces. Second, there is not reasonable expectation of successful combination of the cited references because Chen Cu-Zn alloy techniques may or may not work with Miyafuji Cu alloy sterilization techniques. Third, as stated in the Office Action, the references do not teach or suggest the limitations of herein amended Claims 1 and 11 because as stated in the Office Action, "Chen is silent as to post annealed Cu-Zn alloy being claimed reduced-oxygen Cu-Zn alloy." Thus, primary reference Chen does not provide a reasonable expectation of successful combination that its Cu-Zn alloy will combine with Miyafuji Cu alloy sterilization method. As such, the references cited to reject Applicants claims do not in fact provide an adequate basis for rejection under 35 U.S.C. § 103(a). Thus, Applicants respectfully request the rejections be withdrawn.

Further, the Office Action states:

> In re claim 1, Chen et. al., teach the claimed method of fabricating a semiconductor device, having a reduced-oxygen copper zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising steps of;
>
> - providing a semiconductor substrate having a Cu surface 15 (i.e. a copper seed layer) formed in a via 5 (Fig. 2B);
> - providing a chemical solution (i.e an electroplating solution);
> - electroplating the Cu surface 15 in a chemical solution, thereby forming a Cu-Zn alloy 18 fill in the via 5 and on the Cu surface 15 (Fig. 2C and paragraph [0067]);
> - rinsing the Cu-Zn alloy fill in a solvent (paragraphs [0082] and [0179]);
> - drying the Cu-Zn alloy fill under a gaseous flow (paragraphs [0082] and [0179]);
> - annealing (via a thermal processing step) the Cu-Zn alloy fill 18 formed in the via 5 and on the Cu surface 15 (paragraphs [0069] and [0094], thereby forming a post -annealed Cu-Zn alloy fill;
> - planarizing the post-annealed Cu-Zn alloy fill and the Cu surface 15, thereby completing formation of the post-annealed Cu-Zn alloy filled dual-inlaid interconnect structure (Figs. 2D-2E); and
> - completing formation of the semiconductor device.
>
> Chen et al. is silent as to the post-annealed Cu-Zn alloy being the claimed reduced-oxygen Cu-Zn alloy.

Moreover, contrary to the herein amended Claims 1 and 11, Chen teaches "[o]ne or more contacts 40 are provided to connect the wafer 30 to a plating power supply 45 as a cathode of an electroplating cell" (Para. 0070; Exhibit D). An anode 50 is disposed in the bath 35 and is connected to the plating power supply 45 (Para. 0070). Thus, Chen teaches electroplating a wafer seed using contacts 40, acting as cathodes, which contact one or more locations along the edges of the semiconductor wafer 30. In contrast Claims 1 and 11 positively recite an

electroplating apparatus comprising a cathode-wafer surface where **the cathode-wafer is the Cu surface** (i.e., Specification, p. 4, l. 11, Exhibit A, Fig. 4). In other words, Claims 1 and 11 recite the said electroplating apparatus comprises a cathode-wafer 21 compared to Chen where the physical contacts 40 along the edges of the wafer are the cathodes (Exhibit A; Fig. 4; Exhibit D; Fig. 3). As such, the present invention method is not taught, suggested nor motivated by Chen.

As discussed above, Miyafuji, does not teach, motivate, nor suggest the present invention method, comprising the steps of rinsing and drying the substrate, for **the production of a reduced-oxygen Cu-Zn alloy fill 30 having a uniform zinc distribution along the alloy fill thickness**, as indicated by block 2006 (Specification, p. 11, ll. 29-30). Thus, Chen even in view of Miyafuji, **creates oxidized electroplated metal particles whose size depends on the diffusion depth of the oxygen.** For example, Miyafuji **shows titanium oxide particles formed at the surface are larger than titanium oxide particles formed a depth below the surface** (Fig. 1, Exhibit C).

Thus, Chen, even in view of Miyafuji, does not teach, motivate, nor suggest herein amended independent Claims 1 and 11, respectively reciting:

> 1. **(currently amended)** A method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:
> providing a semiconductor substrate having a Cu surface formed in a via;
> providing a chemical solution;
> electroplating the Cu surface in the chemical solution thereby forming said a Cu-Zn alloy fill in the via and on the Cu surface,
> wherein said electroplating comprises using an electroplating apparatus,
> wherein **said electroplating apparatus comprises:**
> **(a) a cathode-wafer;**
> (b) an anode;
> (c) electroplating vessel; and
> (d) a voltage source, and
> wherein said cathode-wafer comprises a Cu surface,
> rinsing the Cu-Zn alloy fill in a solvent;
> drying the Cu-Zn alloy fill under a gaseous flow;
> annealing the Cu-Zn alloy fill formed in the via and **directly deposited** on the Cu surface, thereby forming **a reduced-oxygen Cu-Zn alloy fill having an alloy surface and an alloy thickness and having a uniform zinc distribution across said alloy surface and said alloy thickness;**
> planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
> completing formation of the semiconductor device.

11. **(currently amended)** A semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by a method comprising the steps of:
providing a semiconductor substrate having a Cu surface formed in a via;
providing a chemical solution;
electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface;
wherein said electroplating comprises using an electroplating apparatus,
wherein **said electroplating apparatus comprises:**
(a) a cathode-wafer;
(b) an anode;
(c) electroplating vessel; and
(d) a voltage source, and
wherein said cathode-wafer comprises a Cu surface,
rinsing the Cu-Zn alloy fill in a solvent;
drying the Cu-Zn alloy fill under a gaseous flow;
annealing the Cu-Zn alloy fill formed in the via and **directly depositing** on the Cu surface, thereby forming **a reduced-oxygen Cu-Zn alloy fill having an alloy surface and an alloy thickness and having a uniform zinc distribution across said alloy surface and said alloy thickness**;
planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and
completing formation of the semiconductor device.

As such, Chen, even in view of Miyafuji, does not teach, motivate, nor suggest the dependent Claims 2, 4, 6, 7, 12, 14, 16, and 17, now subsuming the limitations of the herein amended independent Claims 1 and 11. Therefore, Applicants respectfully request that the Examiner's grounds for rejection be withdrawn and the claims pass to allowance.

IV. Rejection of Claims 8, 9, 18 and 19 under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 8, 9, 18, and 19 under 35 U.S.C. § 103(a), as being unpatentable over Chen et al. (US 2002/008034 A1) ("Chen"), in view of Miyafuji et al. (US 6,313,064) ("Miyafuji"), and in further view of Dublin et al. (US 2002/0084529), stating:

> [ ] Dublin et al. in analogous art (Fig. 6) teach steps of :(1) forming a barrier layer 240 in a via; (2) forming an underlying layer 280A (i.e. a shunt material layer) comprising tin on the barrier layer 240 (paragraphs [0039] and [0031]); (3) forming a Cu surface 290 (i.e. copper seed layer) over the barrier layer 240 and on the underlying layer 280A; and (4) forming an electroplated Cu-Zn alloy 260 on the Cu surface 290. Therefore, one of ordinary skilled in the art, at the time the invention was made, would have been motivated to comprise the underlying layer formed on the barrier layer as taught by Dublin, et. al. and then to proceed the subsequent formation of the Cu-Zn alloy in the via and on the Cu surface as taught by Chen et. al., since by comprising the underlying layer between the barrier layer and the Cu surface it would improve electromigration performance of the semiconductor device. (paragraph [0044], Dublin et al.)

Notwithstanding independent Claims 1 and 11 being herein amended, the Applicants respectfully traverse the Examiner's rejection on this basis.

See supra, The Manual for Patent Examiners' Practice paragraph 2142 requirements for the 103(a) basis for rejection. First, Chen provides a solution for enhancing or repairing ultra-thin or incomplete metal seed layers that have been deposited on the workpiece. Miyafuji, as discussed previously, provides a solution for providing clean environment Cu alloy surfaces where UV light irradiating the Cu alloy surface in hallways sterilizes the Cu alloy surface. Dublin provides a solution for introducing an interconnect structure in an opening through the dielectric over a contact point. Thus, Chen providing a solution for enhancing or repairing ultra-thin metal layers would not be motivated to seek out cited reference Miyafuji that provides sterilized Cu alloy surface or cited reference Dublin providing a solution for introducing an interconnect structure. Second, there is not reasonable expectation of successful combination of the cited references because Chen Cu-Zn alloy techniques may or may not work with Miyafuji Cu alloy sterilization techniques and Dublin's interconnect scheme. Third, the references do not teach or suggest all the limitations of herein amended Claims 1 and 11 because as stated in Office Action, "Chen is silent as to post annealed Cu-Zn alloy being claimed reduced-oxygen Cu-Zn alloy". Thus, Chen does not provide a reasonable expectation of successful combination of its Cu-Zn alloy with Miyafuji Cu alloy sterilization method or Dublin interconnect scheme. As such, the references cited to reject Applicants claims do not in fact provide an adequate basis for rejection under 35 U.S.C. § 103(a).

Moreover, as discussed above, reference Miyafuji produces non-uniform diameter oxidized metal particles along the thickness as such, any combination of references would produce the present Claims 8, 9, and 11 limitations that incorporate features of independent Claims 1 and 11. As such, Claims 8, 9, and 18 should pass to allowance.

V. Rejection of Claim 20 on the Grounds of Non-statutory Double Patenting

The Examiner has rejected Claim 20 on the grounds of non-statutory obviousness-type double patenting, as being unpatentable over Claim 1 of US 6,515,368. This non-statutory obviousness-type double patenting rejection is hereby respectfully traversed, notwithstanding a terminal disclaimer, under 37 C.F.R. § 1.321(c), and a statement, under

37 C.F.R. § 3.73(b), being herewith filed to expedite examination of the present application. Applicants respectfully submit that the interim Cu-Zn alloy thin fill 30 formed on the Cu surface is a patentably distinct feature over the claim 1 Cu-Zn alloy thin film of US 6,515,368. Thus, Claim 20 should pass to allowance.

CONCLUSION

Accordingly, the independent Claims 1 and 11 have been herein amended, notwithstanding the Applicants' belief that application would have been allowable as originally filed. The proposed amendments to the claims are believed to be fully supported by the originally filed Specification. For all the above advanced reasons, Applicants respectfully submit the application is in condition for allowance of the pending claims. Therefore, favorable consideration of the foregoing proposed amendment and remarks is kindly requested. ***The Examiner is further cordially invited to telephone the undersigned for any reason which would advance the pending claims to allowance.***

Respectfully submitted,

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REK/sf
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